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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/690,434	10/18/2000	Masahisa Kobayashi	MA-448-US	3744

30743 7590 05/05/2005

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/690,434	KOBAYASHI, MASAHISA	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20-38 are pending.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 20-38 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by U.S. Patent 6,351,818 to Murai.

4. As to claim 20, Murai discloses a bus power-supply device in a node for connection to a serial bus, said bus power-supply device structured to supply power from a power-supply voltage of a node of a proceeding stage to a node of a next stage through a serial bus connected to said node by a physical layer and a plurality of connectors conductive to each other of the node [FIG. 1, and col. 4, lines 10-21], wherein when a power-supply voltage of said node of the proceeding stage is not supplied, a DC voltage is supplied from said node of the proceeding stage through said serial bus to said physical layer [col. 4, lines 10-16], and when said power-supply voltage is supplied, a DC voltage is supplied from said power-supply voltage to said physical layer by cutting off a path for supplying a DC voltage through said serial bus to said physical layer [col. 3, lines 63-67 and col. 4, lines 1-3].

Murai also discloses that the bus power-supply device may be configured as part of a serial bus interface [FIG. 1, element 3], and that the serial bus interface may be arranged in all of

the nodes connected to the serial bus [col. 4, lines 22-32]. Furthermore, Murai teaches that the serial bus interface is in accordance with the IEEE-1394 standard [col. 1, lines 9-15], which allows for the daisy-chaining of nodes on the bus [col. 1, lines 48-57]. Thus, Murai teaches that communication is maintained between a node and proceeding and next stages through the serial bus whether a power-supply voltage is supplied or not [col. 3, lines 63-67 and col. 4, lines 1-21].

5. As to claim 21, Murai discloses a voltage detection unit which detects said power-supply voltage being supplied or not being supplied [41]; and a selector [42] which supplies a DC voltage coming through said serial bus to said physical layer when said voltage detection unit is yet to detect supply of a power-supply voltage [col. 4, lines 10-16] and supplies a DC voltage from the power-supply voltage to said physical layer by cutting off said path for supplying a DC voltage through said serial bus to said physical layer when said voltage detection unit detects supply [col. 3, lines 63-67 and col. 4, lines 1-3].

6. As to claim 22, Murai discloses said serial bus is an IIEE-1394-1995 Standard serial bus [col. 1, lines 5-7].

7. As to claim 23, Murai discloses a first path for supplying power from said power-supply voltage to said physical layer [2]; and a second path for supplying power coming through said serial bus to said physical layer [100], wherein when power is supplied from said power-supply voltage, said selector cuts off said second path [col. 3, lines 63-67 and col. 4, lines 1-3].

8. As to claim 24, Murai discloses said device comprises a switch [col. 3, lines 30-33]. It is well known to one of ordinary skill in the art that a semiconductor may be used as a switch.

9. As to claim 25, Murai discloses said device comprises a voltage detection unit [col. 3, lines 30-33]. It is well known to one of ordinary skill in the art that a comparator may be used as a voltage detection unit.

10. As to claim 26, Murai discloses said device comprises a voltage detection unit and a selector [col. 3, lines 30-33]. It is well known to one of ordinary skill in the art that a relay element may be used as said voltage detection unit and said selector.

11. As to claim 27, Murai discloses a power-supply circuit [2] which converts said power-supply voltage into a DC voltage for said serial bus and outputs said DC voltage; a converter [4] which converts a DC voltage output from said power-supply circuit into a DC voltage for said physical layer; a voltage detection unit [41] which detects said power-supply voltage being supplied or not being supplied to said power-supply circuit; and a selector [42] which supplies a DC voltage applied through said serial bus to said converter when said power-supply voltage is not supplied to said power-supply circuit and cuts off a path for supplying a DC voltage through said serial bus to said converter to supply an output of said power-supply circuit to said converter when said power-supply voltage is supplied [col. 3, lines 63-67 and col. 4, lines 1-17].

12. As to claim 28, Murai discloses a first path for supplying power from said power-supply voltage to said physical layer [2]; and a second path for supplying power coming through said serial bus to said physical layer [100], wherein when power is supplied from said power-supply voltage, said selector cuts off said second path [col. 3, lines 63-67 and col. 4, lines 1-3].

13. As to claim 29, Murai discloses said voltage detection unit detects said power-supply voltage being supplied or not being supplied by detecting an output voltage of said power-supply circuit [col. 3, lines 63-67 and col. 4, lines 1-3].

14. As to claim 30, Murai discloses said voltage detection unit [41] detects said power-supply voltage being supplied or not being supplied by detecting an output voltage of said power-supply circuit, and which further comprises a first path for supplying power from said power-supply voltage to said physical layer [2]; and a second path for supplying power coming through said serial bus to said physical layer [100], wherein when power is supplied from said power-supply voltage, said selector cuts off said second path [col. 3, lines 63-67 and col. 4, lines 1-3].

15. As to claim 31, Murai discloses a first path for supplying power from said power-supply voltage to said physical layer [2]; and a second path for supplying power coming through said serial bus to said physical layer [100], wherein when power is supplied from said power-supply voltage, said selector cuts off said second path [col. 3, lines 63-67 and col. 4, lines 1-3]. Furthermore, it is well known to one of ordinary skill in the art that a semiconductor may be used as a switch.

16. As to claim 32, Murai discloses said voltage detection unit detects said power-supply voltage being supplied or not being supplied by detecting an output voltage of said power-supply circuit [col. 3, lines 63-67 and col. 4, lines 1-3]. Furthermore, it is well known to one of ordinary skill in the art that a semiconductor may be used as a switch.

17. As to claim 33, Murai discloses said device comprises a voltage detection unit [col. 3, lines 30-33]. It is well known to one of ordinary skill in the art that a comparator may be used as a voltage detection unit.

18. As to claim 34, Murai discloses said device comprises a voltage detection unit and a selector [col. 3, lines 30-33]. It is well known to one of ordinary skill in the art that a relay element may be used as said voltage detection unit and said selector.

19. As to claim 35, Murai discloses a node having a bus power-supply device in a node for connection to a serial bus, said bus power-supply device structured to supply power from a power-supply voltage to a node of a next stage through a serial bus connected to said node by a physical layer and a plurality of connectors conductive to each other of the node [FIG. 1, and col. 4, lines 10-21], comprising: a plurality of connectors each having a power-supply terminal to which a DC voltage is applied from other nodes through said serial bus and a signal terminal to and from which a signal from other nodes in input and output [100, 111, 112, 113]; a physical layer [6] which outputs a signal input through a signal terminal of one connector to a signal

terminal of the other connector, wherein power-supply terminals of said plurality of connectors are rendered conductive to each other, said bus power-supply device supplies a DC voltage through said serial bus to said physical layer through said power-supply terminal when none of a power-supply voltage of said node is supplied [col. 4, lines 10-16], and supplies a DC voltage from the power-supply voltage to said physical layer by cutting off a path for supplying a DC voltage through said serial bus to said physical layer when said power-supply voltage is supplied [col. 3, lines 63-67 and col. 4, lines 1-3].

Murai also discloses that the bus power-supply device may be configured as part of a serial bus interface [FIG. 1, element 3], and that the serial bus interface may be arranged in all of the nodes connected to the serial bus [col. 4, lines 22-32]. Furthermore, Murai teaches that the serial bus interface is in accordance with the IEEE-1394 standard [col. 1, lines 9-15], which allows for the daisy-chaining of nodes on the bus [col. 1, lines 48-57]. Thus, Murai teaches that communication is maintained between a node and proceeding and next stages through the serial bus whether a power-supply voltage is supplied or not [col. 3, lines 63-67 and col. 4, lines 1-21].

20. As to claim 36, Murai discloses said bus power-supply device comprises a voltage detection unit [41] which detects said power-supply voltage being supplied or not being supplied; and a selector [42] which supplies a DC voltage coming through said serial bus to said physical layer when said voltage detection unit is yet to detect supply of a power-supply voltage [col. 4, lines 10-16] and supplies a DC voltage from the power-supply voltage to said physical layer by cutting off said path for supplying a DC voltage through said serial bus to said physical layer when said voltage detection limit detects supply [col. 3, lines 63-67 and col. 4, lines 1-3].

21. As to claim 37, Murai discloses a first path for supplying power from said power-supply voltage to said physical layer [2]; and a second path for supplying power coming through said serial bus to said physical layer [100], wherein when power is supplied from said power-supply voltage, said selector cuts off said second path [col. 3, lines 63-67 and col. 4, lines 1-3].

22. As to claim 38, Murai discloses said bus power-supply device comprises a power-supply circuit [2] which converts said power-supply voltage into a DC voltage for said serial bus and outputs said DC voltage; a converter [4] which converts a DC voltage output from said power-supply circuit into a DC voltage for said physical layer; a voltage detection unit [41] which detects said power-supply voltage being supplied or not being supplied to said power-supply circuit; and a selector [42] which supplies a DC voltage applied through said serial bus to said converter when said power-supply voltage is not supplied to said power-supply circuit [col. 4, lines 10-16] and cuts off a path for supplying a DC voltage through said serial bus to said converter to supply an output of said power-supply circuit to said converter when said power-supply voltage is supplied [col. 3, lines 63-67 and col. 4, lines 1-3].

Response to Arguments

23. Applicant's arguments filed February 4, 2005 have been fully considered but they are not persuasive.

24. In the remarks, applicants argued in substance that Murai only shows a computer system having two attached devices and does not teach or suggest devices connected in a serial bus line. But Murai also discloses that the bus power-supply device may be configured as part of a serial bus interface [FIG. 1, element 3], and that the serial bus interface may be arranged in all of the nodes connected to the serial bus [col. 4, lines 22-32]. Furthermore, Murai teaches that the serial bus interface is in accordance with the IEEE-1394 standard [col. 1, lines 9-15], which allows for the daisy-chaining of nodes on the bus [col. 1, lines 48-57]. Thus, Murai teaches that communication is maintained between a node and proceeding and next stages through the serial bus whether a power-supply voltage is supplied or not [col. 3, lines 63-67 and col. 4, lines 1-21].

25. In the remarks, applicants argued in substance that Murai does not teach or suggest the presence or absence of internal power supplies of the two devices. But Murai teaches that devices with an IEEE-1394 interface are powered by a power source within itself [col. 1, lines 58-63].

26. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., devices having power supplies of differing voltages) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

April 29, 2005
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